NASA Electronic Parts and Packaging Program (NEPP)

Reliability of Tantalum Capacitors

Effect of Inductance and Requirements for Surge Current Testing of Tantalum Capacitors

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Abstract.

Surge current testing is considered one of the most important techniques to evaluate reliability and/or screen out potentially defective tantalum capacitors for low-impedance applications. Analysis of this test, as it is described in the MIL-PRF-55365 document, shows that it does not address several issues that are important to assure adequate and reproducible testing. This work investigates the effect of inductance of the test circuit on voltage and current transients and analyzes requirements for the elements of the circuit, in particular, resistance of the circuit, inductance of wires and resistors, type of switching devices, and characteristics of energy storage bank capacitors. Simple equations to estimate maximum inductance of the circuit to prevent voltage overshooting and minimum duration of charging/discharging cycles to avoid decreasing of the effective voltage and overheating of the parts during surge current testing are suggested.

I. Introduction.

High current spikes caused by power supply transients might result in short-circuit failures of tantalum capacitors and cause catastrophic consequences for electronic systems, including igniting the system. The probability of this type of failure is especially high for low-impedance circuits when inrush currents are limited mostly by the impedance of the capacitor itself [1]. Recently, these problems have gained yet more importance due to proliferation of distributed-power architecture systems and low-voltage DC-DC converters.

Failures due to surge currents always have been a serious concern for manufacturers of tantalum capacitors and for design engineers. To bound inrush currents, application of limiting resistors was strongly recommended. First, in the 1960s, the requirement was 3 Ohms per each volt of operating voltage, but by the 1980s, due to improvement in reliability of the parts and strong commercial need to increase the efficiency of power supply systems, this requirement was reduced to 1 Ohm and in the 1990s even to 0.1 Ohm per volt [2, 3]. To further assure reliable operation of tantalum capacitors in low-impedance applications, derating of the voltage to 50% and even 25% of the capacitor's rated voltage is recommended [1]. However, in [4, 5] the authors argue that this rule for derating is not necessarily correct for new high-quality products.

These trends clearly indicate a tendency of both designers and manufacturers to further decrease minimal values of limiting resistors and to relax requirements for derating, thus increasing operating voltages of tantalum capacitors in low-impedance applications. In this situation, it is important to have a clearly understood and proven methodology allowing reproducible and reliable evaluation of performance of the capacitors under high surge current stress conditions.

The capability of tantalum capacitors to withstand high current transients is evaluated during surge current testing described for chip tantalum capacitors in the MIL-PRF-55365 standard. For hermetically sealed tantalum capacitors, similar test (with some minor variations) is described in MIL-PRF-39003. Surge current testing according to these standards is also recommended to screen out potentially weak parts for high-reliability space applications [6].

According to MIL-PRF-55365, the part is subjected to 10 surge cycles in a circuit similar to the one shown in Figure 1. Each cycle includes charging a bank energy storage capacitor, $C_{B,}$ to the rated voltage for 4 seconds and then discharging it to the device under test for 4 seconds and changing the switch to the upper position. The purpose of capacitor C_B, which is required to be not less than 50,000 μF, is to simulate a power supply with low impedance. The standard requires that the total DC resistance of the circuit, R_C, including the wiring, fixturing, and output impedance of the power supply, shall be a maximum of 1.2 Ohms.

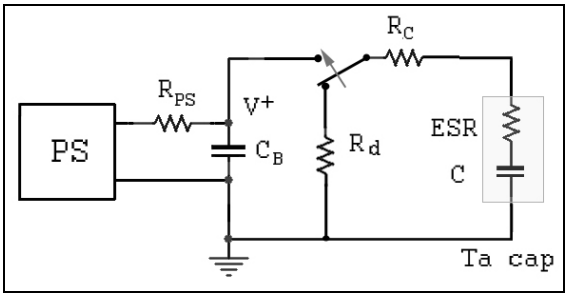


Figure 1. A simplified schematic of the surge current test per MIL-PRF-55365.

Some authors [2, 7, 8] have indicated that inductance of the circuit might increase the probability of failures during surge current testing. However, no analyses of conditions that would cause failures and/or requirements to limit the value of the inductance have been given.

The purpose of this work is to evaluate inductance of elements of the circuit, analyze the effect of inductance during surge current testing, discuss requirements for components used, and analyze test conditions to assure more adequate and reproducible results. Analysis of failure mechanisms in tantalum capacitors caused by high current spikes is out of the scope of this work and will be discussed in a separate paper.

Contents of this paper:

II. Inductance of elements of the test circuit.

II.1. Inductance of capacitors.

Frequency dependencies of impedance, Z, of tantalum capacitors have a so-called self-resonance frequency, f_r, at which the impedance reaches minimum. The value of f_r for these parts is considered to be in the range from 0.2 to 1 MHz [9]; however, recent data indicate that f_r might be as high as 2 to 3 MHz [10].

The behavior of Z-f characteristics can be explained assuming that the equivalent circuit of a tantalum capacitor can be represented as a capacitor, inductor, and resistor connected in series. For this circuit the impedance Z and its modulus |Z| can be calculated as:

$$Z = (ESR) + j\omega(ESL) - \frac{j}{\omega C}$$

$$|Z| = \sqrt{(ESR)^2 + \left(\omega \times (ESL) - \frac{1}{\omega \times C}\right)^2},$$

where ω is the radian frequency and ESR and ESL are the effective series resistance and inductance of the capacitor, respectively. The self-resonant frequency can be defined as:

$$f_r = \frac{1}{2\pi \times \sqrt{C \times (ESL)}}.$$

At relatively low frequencies, $f < f_r$, the part behaves as a capacitor, and at $f > f_r$ as an inductor.

Ceramic capacitors show similar characteristics and also have self-resonant frequencies, which are typically greater compared to tantalum capacitors. This is due to both lower C and lower ESL values of ceramic parts. An overview of inductive properties of different types of low-voltage capacitors is given by Ewell [11]. An increasing need for decoupling of signals in advanced high-frequency microcircuits and processors stimulated multiple theoretical and experimental studies of inductance characteristics of chip ceramic capacitors. Typically, the inductance of these parts varies from 4 to 5 nanohenries (nH) for leaded [12] to 1.1 to 1.7 nH for 2225-style chip capacitors [13], to 0.18 nH for 1206-style capacitors [14], and to 0.4 – 0.9 nH for 0805-style capacitors [11]. Special-design, small-value ceramic capacitors might have inductance as low as 50 pH [15].

Much less is known about the inductance of tantalum capacitors. According to Derksen at al. [16], both chip ceramic and tantalum capacitors have similar inductance in the order of 1-3 nH depending on their size. However, Martin [17], using a fast edge rate current pulse technique, has shown that 0.1 μF ceramic capacitors have 2.5 times less inductance compared to the same nominal tantalum capacitors, which had L ~ 12.5 nH. This value is consistent with 10.9 nH for 5.6 μF low ESR tantalum capacitors reported in [11]. Similar to chip ceramic capacitors, ESL

values of tantalum capacitors do not correlate with values of capacitance and/or rated voltage and remain within relatively narrow limits for a given size of the parts [18]. However, inductive characteristics of tantalum chip capacitors have not been studied properly yet and there are no specifications for ESL measurements.

The inductance of a capacitor consisting of two parallel plates of width *W*, length *l*, and distance between the plates *d*, can be calculated as [19]:

$$L = \mu\mu_0 \frac{d \times l}{W},$$

where $\mu_o = 1.26\times10^{-6}$ H/m is the permeability of free space and μ is the permeability of the dielectric.

Note that according to this equation, for a given value of the capacitor diminishing of the length *l* (the size along the current flow) and increasing of the width, *W* would reduce *L*. This is an effective means for reduction of inductance in application of ceramic capacitors [11].

Considering that for a tantalum pentoxide dielectric $\mu \approx 1$ and the effective area typically is ~100 cm^2 and $d \sim 0.1$ μm, for rough estimations it is possible to assume l = 1,000 mm and W = 10 mm. At these conditions calculations yield $L \approx 13$ pH. This is an extremely small value, and even considering inductance of the terminals, which typically does not exceed one nanohenry, the discrepancy between the calculations and experimental data remains rather significant. It is quite possible that the heterogeneity of the cathode and, in particular, micro-irregularities in the conductivity of the manganese layer, do not allow for identical distribution of the current density in tantalum and manganese electrodes, so that the magnetic field outside the capacitor is not compensated completely. This might increase the inductance and cause higher ESL values of tantalum capacitors compared to ceramic parts of a similar size.

A simple method for ESL evaluation would be direct measurements of frequency dependencies of active and reactive resistances of the part. In our experiments these measurements were carried out in the range of frequencies from 0.1 kHz to 10 MHz on several CWR09-style capacitors using an impedance analyzer HP4192A with a direct coupled test fixture. Calculations based on these experiments showed that the inductance increases with frequency and levels off at *f* above ~ 2 MHz resulting in ESL varying from 80 nH to 110 nH. However, during discussion with Erik Reed (JPL), he has indicated that these values are not consistent with the data obtained by direct measurements of high-frequency impedance for these parts and suggested a simple technique for ESL assessment.

Figure 2 shows a schematic for Z-f measurements using a high-frequency generator with the output limited by a 50-Ohm resistor and oscilloscope connected directly to the terminals of the capacitor with short coaxial cables.

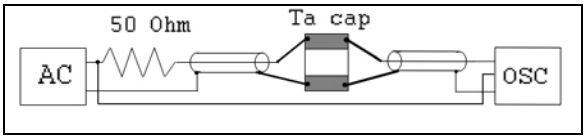


Figure 2. A set-up for measurements of high-frequency characteristics of tantalum capacitors.

Measurements of the input and output signals allowed for the phase shift and impedance calculations. Results of these calculations for two T495X156M050AS capacitors in the rage of frequencies from 1 kHz to 20 MHz are shown in Figure 3. Assuming that in the range from 3 to 6 MHz the impedance is mostly related to the inductance of the part and the skin effect is negligible, so that $|Z| = \omega \times L$, the calculated ESL values are in the range from 2.5 to 3 nH. These values are far below those obtained with hp4192A measurements and match the data reported by the manufacturer [10].

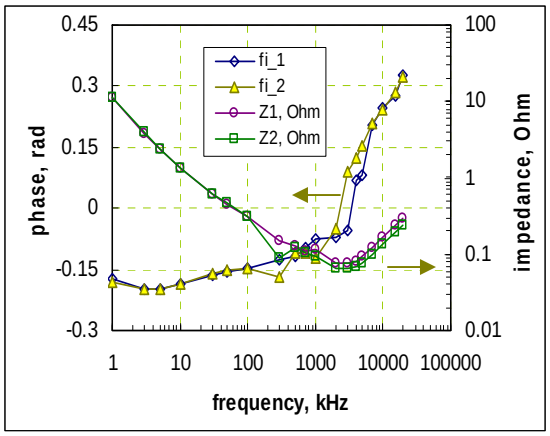


Figure 3. Frequency dependence of the impedance and phase shift for two T495X156M050AS capacitors.

The discrepancy compared to the results obtained using the impedance analyzer is presumably due to parasitic inductance and inadequate compensation of the fixture used for HP4192A measurements. Based on the available data, ESL of chip tantalum capacitors are likely in the range from 2 to 15 nH with higher values corresponding to larger-sized parts.

II.2. Inductance of wires and resistors.

Wires connecting elements of the circuit also have inductance, which can be calculated as [20]:

$$L_W = 2 \times l \times \left[\ln\left(\frac{2l}{r}\right) - 0.75 \right],$$

where L_W is the low-frequency inductance of a straight piece of wire in nanohenries, l is the length of the wire in cm, and r is the radius of the wire in cm. Figure 4 shows variations of the L_W with the length for different wire diameters (AWG).

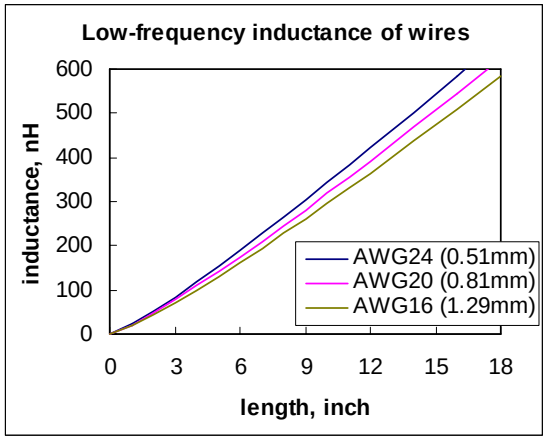


Figure 4. Variation of the inductance with length for wires of different diameters.

A total effective length of all wires used should be taken into account when the inductance of the testing circuit is estimated. A total effective length of the wire in a typical surge current test circuit can vary from 6 inches to ~1.5 feet, which would result in inductance varying from ~150 nH to ~600 nH. Testing of the parts in temperature chambers might require even longer wires, up to 2 to 2.5 feet, and would result in higher inductances, up to 900 or 1,200 nH.

Power wire-wound resistors, which might be used to limit inrush currents during the surge testing, also have relatively high inductances. Measurements of several power resistors of 1 Ohm nominal gave inductances varying from 150 to 300 nH.

Estimations show that the inductance of the external circuit used for surge current testing, L_c, can vary from ~150 nH to ~1,500 nH.

III. Transients during surge testing.

The rise time of transients during surge current testing is in the microsecond range, which corresponds to the megahertz range in the frequency domain. For this reason, the inductance of capacitors cannot be neglected, and the equivalent circuit of the part should be represented as a capacitor, resistor, and inductor connected in series. Considering also inductance of external elements of the circuit, the schematic of the test shown in Figure 1 should be replaced with the circuit shown in Figure 5.

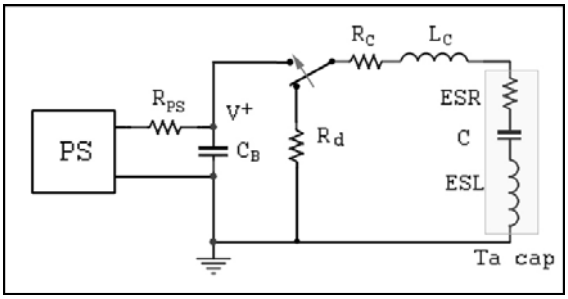


Figure 5. A schematic of the surge current test with consideration of inductance.

Transients in a circuit consisting of a capacitor C, inductor L, and resistor R, connected in series to a power supply V_0 are described thoroughly in many handbooks on electrical circuits and can be calculated using the following differential equations:

$$LC\frac{d^2u}{dt^2} + RC\frac{du}{dt} + u = V_0 \tag{1}$$

$$i(t) = C\frac{du}{dt}, \tag{2}$$

where *u(t)* is the voltage across the capacitor *C* and *i(t)* is the current through the part. For the circuit shown in Figure 5, $R = ESR + R_c$ and $L = ESL + L_c$. Because the bank energy storage capacitor C_B is much larger than the capacitance of device under test, *C*, the total capacitance of the circuit is equal to *C* with sufficient accuracy.

When a switch in Figure 5 is turned to charge an initially discharged tantalum capacitor at *t = 0*, the initial conditions are: *u(0) = 0*, because the voltage across a capacitor cannot change instantaneously, and *i(0) = 0*, because the current through an inductor cannot change instantaneously either.

Solutions to this R-C-L model, Eq. (1) and (2), at different conditions were obtained based on Heviside's operational method [21] and are analyzed below.

III.1. Overdamped conditions.

These conditions occur at relatively low *L* and high *R* and *C*, when parameter *b* is a real number:

$$b^2 = \left(\frac{R}{2L}\right)^2 - \frac{1}{LC} > 0. \tag{3}$$

In this case the voltage *u(t)* changes with time smoothly from 0 to V_0 and the solution to (1) can be expressed using hyperbolic functions:

$$u = V_0\left[1 - e^{-at}\left\{\cosh(bt) + \frac{a}{b}\sinh(bt)\right\}\right] \tag{4}$$

$$i = \frac{V_0}{Lb}e^{-at}\sinh(bt), \tag{5}$$

where *a = R/(2L)* is the so-called damping coefficient.

III.2. Underdamped conditions.

These conditions occur at relatively high L and low resistance and capacitance of the circuit when a self-resonance frequency, $\omega_0 = (1/LC)^{0.5}$, exceeds the damping coefficient and parameter ω is a real number:

$$\omega^2 = \frac{1}{LC} - \left(\frac{R}{2L}\right)^2 > 0. \tag{6}$$

In this case the voltage and current exhibit oscillations as they settle with time to steady-state conditions passing through extreme values. The solution to (1) gives attenuated oscillations and can be expressed through trigonometric functions:

$$u = V_0\left[1 - e^{-at}\left\{\cos(\omega t) + \frac{a}{\omega}\sin(\omega t)\right\}\right] \tag{7}$$

$$i = \frac{V_0}{L\omega}e^{-at}\sin(\omega t)\,. \tag{8}$$

III.3. Critical damping condition.

If parameters *b* and ω are equal to zero, the solution is simplified and can be written as follows:

$$u = V_0\left[1 - e^{-at}(1 + at)\right] \tag{9}$$

$$i = \frac{V_0 t}{L}e^{-at}\,. \tag{10}$$

This condition occurs only rarely and is not very important from a practical perspective.

III.4. R-C model.

Transients in cases when both inductances of the capacitor and of the circuit are negligibly small can be calculated using a simple R-C model:

$$u = V_0\left(1 - e^{-t/\tau}\right) \tag{11}$$

$$i = \frac{V_0}{\left(ESR + R_c\right)} \times e^{-t/\tau}\,, \tag{12}$$

where the time constant $\tau = (ESR+R_c)\times C$.

III.5. Comparison with experiment.

To evaluate how close the results of theoretical simulations are to the real transients, a current spike through a 15 μF/50 V tantalum capacitor with ESR = 0.08 Ohm was measured using a Tektronix AM503 current probe amplifier during surge current testing in a circuit with the effective length of the wires at ~9 inches. The estimated inductance of this circuit $L_c \approx 250$ nH and resistance $R_c \approx 0.2$ Ohm. Interestingly, a slight variation of characteristics of the circuit used for simulations resulted in changes between overdamped, Eq. (5), and underdamped, Eq. (8), conditions; however, results of these calculations were similar. Current transients calculated according to R-C-L and R-C models together with experimental measurements are shown in Figure 6. It is seen that the R-C-L model displays much better agreement with the experimental data compared to the R-C model.

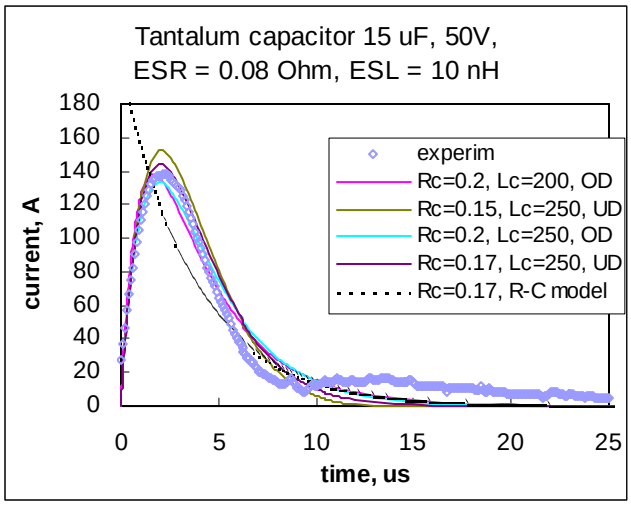
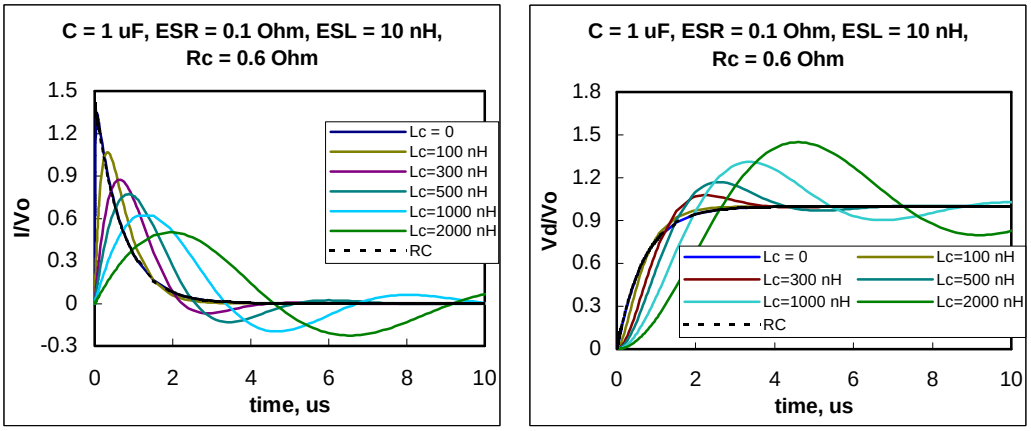


Figure 6. Experimental and calculated transients in a 15 μF, 50 V tantalum capacitor. The legend indicates values of R_c and L_c used for calculations according to the R-L-C and R-C models. OD and UD means overdamped and underdamped conditions in the R-L-C model.

IV. Analysis of transients.

IV.1. Effect of inductance.

As an example of the effect of inductance on transients, Figure 7 shows results of a simulation of surge current testing calculated according to Eq. (4), (5), (7), and (8) for a capacitor under test having C = 1 μF, ESR = 0.1 Ohm, and ESL = 10 nH. The external resistance of the circuit, Rc = 0.6 Ohm, and inductance is assumed to vary from 0 to 2 μH. The charts show also transients calculated using a simple R-C model.



a) b)

Figure 7. Simulation of current (a) and voltage across the dielectric (b) transients during surge testing for a 1 μF capacitor at different values of circuit inductance L_c. The resistance of the circuit, R_c = 0.6 Ohm, was chosen in the middle of the range allowed per MIL-PRF-55365.

It is seen that increasing inductance in the circuit has three major effects:

1. A decrease in the amplitude of current spike, I_{sp}. The value of I_{sp} decreases more than 40% as the circuit inductance increases from 0 to 500 nH and more than 60% at L_c = 2,000 nH.
2. An increase in the time to maximum, τ_{max}, and duration of the current spike, τ_{sp}. The value of τ_{sp} can be estimated as the width of the I(t) curve at $I = 0.5 \times I_{sp}$. For the 1 μF capacitor, an increase of L_c from 0 to 1,000 nH increases τ_{sp} from 0.5 μs to 2.2 μs and τ_{max} from 0.05 μs to 1.5 μs.
3. An increase of the possibility of voltage overshooting. As inductance of the circuit increases, the voltage transient transforms from the overdamped to underdamped condition, which results in oscillations and increase of the voltage across the capacitor to values above the nominal (or applied) voltage, V_0.

This overshooting might be rather substantial and, for the considered case, the voltage amplitude increases more than 20% at L_c above ~500 nH and more than 45% above 2,000 nH. This might result in breakdown of the capacitor. Overshooting up to 70% has been observed experimentally in a set-up used by H. Holland [8] and increased significantly the rate of failures during surge current testing.

A decrease of I_{sp} with increasing inductance goes along with increase of τ_{sp}, so that the total energy dissipated in the capacitor remains constant. However, instantaneous rise of the current might result in adiabatic local overheating, causing damage to the electrodes and dielectric and failure of the part. It is quite possible that at lower and wider current spikes this condition would not have been reached. The effect of inductance-induced variations of the shape of current spikes on the results of surge current testing requires additional analysis. However, the implications of overshooting are quite obvious: increased probability of capacitors' breakdown and failures. In any case, different test laboratories using different surge current test set-ups might have different failure rates due to uncontrolled inductance of the circuits.

A simple Visual Basic program was developed to calculate variation of the three major parameters characterizing surge current testing: I_{sp}, τ_{sp}, and overshooting (V_{max}/V_0), versus parameters of the circuit (L_c, R_c) and of the part (C, ESR, ESL). Results of these calculations for two types of capacitors are shown in Figure 8. One capacitor had C = 1 μF, ESR = 0.05 Ohm, and ESL = 5 nH, and another had C = 15 μF, ESR = 0.1 Ohm, and ESL = 10 nH. Note that the current spike amplitudes shown in Figures 8a and 8b are normalized to 1 V of applied voltage.

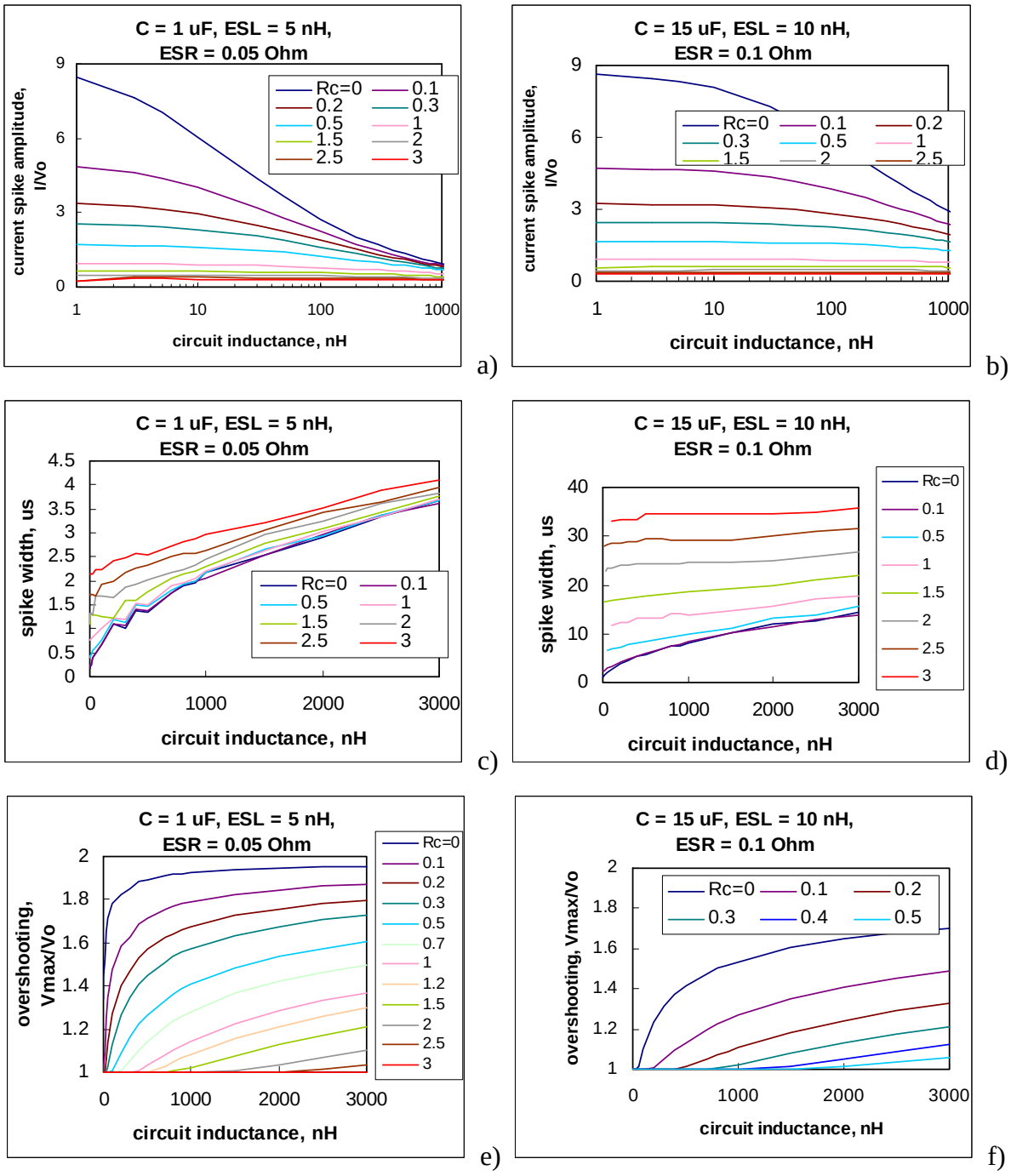


Figure 8. Effect of inductance and resistance of the circuit on the amplitude of current spike (a, b), spike duration (c, d), and overshooting (e, f) for a 1 μF (a, c, e) and 15 μF (b, d, f) capacitors. The legend shows values of R_c in Ohms.

It is seen that the effect of inductance is especially significant for circuits with low resistances. At $R_c = 0$ an increase of L_c from 0 to 500 nH almost five times decreases I_{sp} for a 1 μF capacitor, whereas at $R_c = 1.2$ Ohms (maximum external resistance per MIL-PRF-55365) this decrease was ~ 40% only.

Contrary to the R-C model, in which the amplitude of current spike depends on ESR and R_c only, see Eq. (12), for the R-C-L model I_{sp} depends also on the value of the capacitor. For example, at L_c = 500 nH and R_c in the range from 0.2 Ohm to 1 Ohm, I_{sp} for a 15 μF capacitor is 2.1 to 1.3 times greater than for a 1 μF capacitor.

The pulse width increases virtually linearly with the external inductance and has a relatively weak dependence on R_c for 1 μF capacitors but varies much more significantly for 15 μF parts.

As expected, overshooting increases with an increase of inductance and decrease of resistance of the circuit. For example, for 1 μF parts at R_c = 0.1 Ohm, the overshooting increases from 5% at L_c = 0 to ~85% at L_c = 1 μH. Theoretically, at large enough L_c, the voltage would oscillate with amplitude of V_0 around an average value of V_0, thus resulting in voltage across the capacitor rising up to $2\times V_0$. These results indicate that the inductance-induced overshooting might be a major reason for failures during surge current testing and that the value of external inductance of the circuit should be limited to assure adequate and reproducible results of testing.

It is quite possible that in practice, when a low-impedance circuit operates with a load having a large enough inductance, overvoltage conditions on a tantalum capacitor would occur. For these cases it is reasonable to evaluate the capability of the part to withstand short, microsecond-level voltage spikes up to two times the rated voltage. This might necessitate development of a special "surge voltage" testing, which would require different test conditions compared to the existing surge current testing.

IV.2. Effect of resistance.

The effect of external resistance in the circuit on results of surge current testing of tantalum capacitors has been shown experimentally by Holland [8] and Reed and Paulsen [3]. According to [3], the dependence of breakdown voltage on the circuit resistance follows a power law, $V_B = \alpha R_c^{\beta}$ with an exponent $\beta \sim 0.2$. Interestingly, simulations of surge testing at underdamped conditions for 1 μF and 15 μF capacitors gave variations of maximum voltage values with R_c that can be approximated with a power law also (see Figure 9). The exponent, calculated for voltage overshooting using the least-square-fit method, varied from 0.23 to 0.26 for 1 μF capacitors and from 0.13 to 0.15 for 15 μF parts, which is reasonably close to the results of Reed and Paulsen.

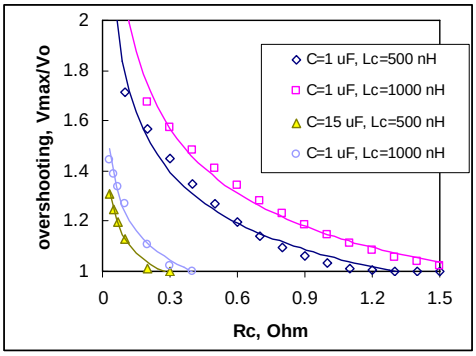
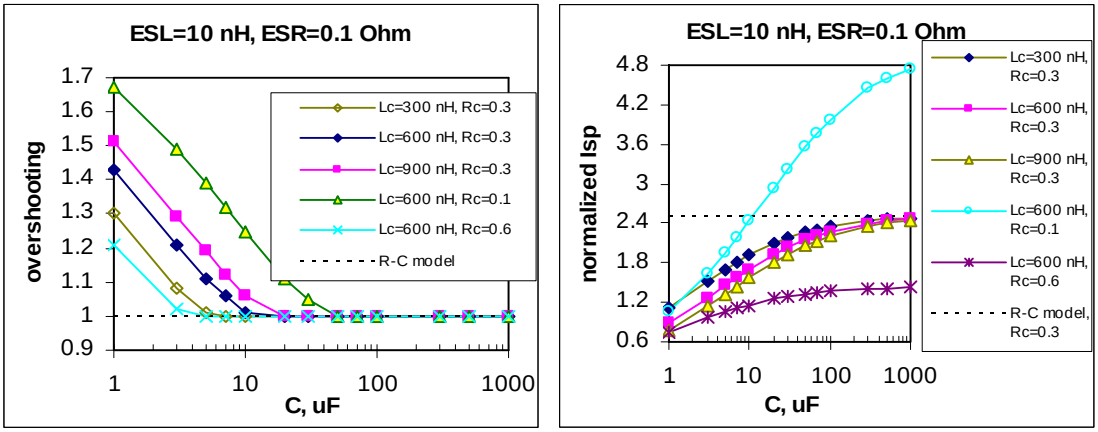


Figure 9. Effect of circuit resistance on voltage overshooting for 1 μF and 15 μF capacitors at L_c = 500 nH and L_c = 1,000 nH. Marks indicate results of calculations per R-C-L model and lines indicate approximations with a power law.

IV.3. Effect of capacitance.

According to a simplified R-C model, see Eq. (11), the voltage across a tantalum capacitor during the test gradually increases to V_0 and no voltage overshooting occurs. The amplitude of a current spike is inversely proportional to the total resistance of the circuit and does not depend on the value of capacitance. However, the R-C-L model predicts significant variations of I_{sp} and overshooting with capacitance. Figure 10 shows calculated dependence of the overshooting and current spike amplitude on the value of the capacitor under test. It was assumed that all capacitors have ESR = 0.1 Ohm and ESL = 10 nH. Inductance of the circuit, L_c, varied from 300 nH to 900 nH and resistance, R_c, from 0.1 to 0.6 Ohm.



a) b)

Figure 10. Effect of capacitance on overshooting (a) and current spike amplitude (b) according to R-C-L model. Dashed lines are results of calculations per R-C model.

Figure 10 shows that for a circuit with R_c = 0.3 Ohm and L_c = 600 nH, an increase in capacitance from 1 μF to 20 μF decreases overvoltage from 42% to 0. The amplitude of current spikes at these conditions increases more than two times. A decrease in R_c to 0.1 Ohm makes these variations even more significant: overvoltage decreases from 67% to 10 % and I_{sp} increases approximately 2.8 times.

This simulation shows that results of surge current testing carried out on the same set-up on capacitors rated to the same voltage, V_0, depend on the value of the capacitor under test. Capacitors of greater values would experience less voltage overshooting but higher current spikes compared to lower value parts. This might result in variations of failure mechanisms and the probability of breakdown depending on the value of a capacitor. For example, low-value capacitors might fail predominantly due to electrical breakdown of tantalum pentoxide, whereas high-value capacitors more likely would fail due to local overheating of the manganese cathode layer.

V. Requirements for surge current testing.

For surge current testing of tantalum capacitors MIL-PRF-55365 standard specifies only a value of the bank capacitor, C_B (50,000 μF minimum), the sum of DC resistance of wiring, fixturing, and output impedance of the power supply, R_c (1.2 Ohms maximum). The charging cycle is

required to be 4 seconds ±1 second, and the discharging time should be also 4 seconds ±1 second to a voltage below 1 percent of rated voltage per the standard.

Below is a brief analysis of these requirements and other factors that have not been addressed in the standard, but might affect results of the testing and are important to assure reproducible results.

V.1. External resistance of the circuit.

The MIL-PRF-55365 standard defines resistance of the circuit, R_c, as a sum of DC resistance of circuit elements and impedance of power supply, which is ambiguous because impedance is a function of frequency, and the frequency is not specified. It is assumed to be likely that impedance of the capacitor C_B is considered when impedance of the regulated power supply is calculated; however, it is not clearly stated in the document. To avoid uncertainty, it is reasonable to replace the words "output impedance of the regulated power supply" in the standard with "ESR of the energy storage bank capacitor."

As was shown above, variations of R_c within the permissible range of 0 Ohm to 1.2 Ohm significantly change the level of overshooting and shape and amplitude of current spikes. These variations affect also the proportion of energy, *Q*, which is dissipated in the capacitor.

The energy dissipated in a tantalum capacitor does not depend on inductance of the circuit, so for simplicity, the R-C model, see Eq. (11) and (12), is used for calculations. For a circuit with an external resistor R_c, the energy dissipated during surge current testing of a capacitor C with resistance ESR can be expressed as follows:

$$Q = \int_0^\infty i^2 \times (ESR) \times dt = \frac{V^2 \times (ESR)}{\left[R_c + (ESR)\right]^2} \int_0^\infty \exp\left(-2t/\tau\right) \times d\tau \,, \qquad (13)$$

The integration yields:

$$Q = \frac{C \times V^2}{2} \times \frac{(ESR)}{\left[R_c + (ESR)\right]} = \alpha \times \frac{C \times V^2}{2} \,, \qquad (14)$$

where $\alpha = (ESR)/[R_c+(ESR)]$ is the coefficient indicating the proportion of energy dissipated in the capacitor.

For a typical capacitor with ESR = 0.1, α varies from 100% at R_c = 0 to 7% only at R_c = 1.2 Ohms. Obviously, laboratories using test set-ups with different R_c might produce different results of the surge current testing by discharging different energy in the part. For this reason, allowable R_c values should be limited to a narrower range, for example from 0.5 Ohm to 1 Ohm. At these conditions α would typically change in a relatively narrow range from 17% to 9% only. Setting a limit to the minimal R_c value would also significantly reduce the possibility of overshooting in capacitors by relaxing the requirements to maximum inductance in the circuit.

Unfortunately, the value of R_c is difficult to estimate accurately enough and it would be not easy to maintain R_c within the tighter limits. However, the amplitude and shape of current spikes, which directly depend on R_c, can be measured relatively easily using a current probe or a small-value current shunt resistor connected in series with the capacitor under test. Using current spike oscillograms, the effective values of R_c could be estimated and these values and/or the

oscillograms should be reported together with the results of surge current testing for reference purposes.

V.2. External inductance of the circuit.

To avoid oscillations and voltage overshooting during the surge testing, the external elements of the circuit should have values, which would provide overdamping conditions of the transient. By introducing a critical inductance, L_{cr}, which is calculated per Eq. (15), the requirement of Eq. (3) can be satisfied if $L = L_c + ESL < L_{cr}$ for a given external resistance of the circuit, R_c, and values of C and ESR of the capacitor.

$$L_{cr} = \frac{C \times (R_c + ESR)^2}{4}. \qquad (15)$$

The dependence of L_{cr} on total resistance, $R = R_c + ESR$, for capacitors varying from 1 μF to 1,000 μF is shown in Figure 11.

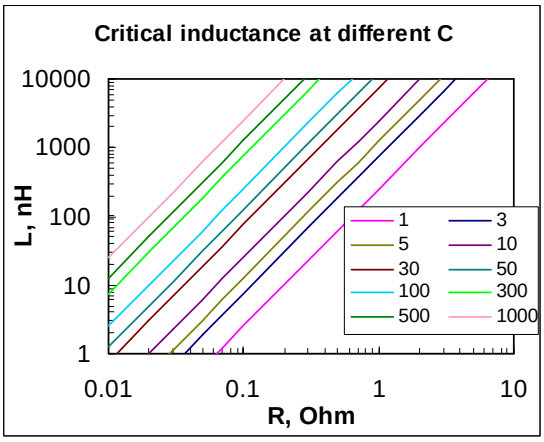


Figure 11. Critical inductance vs. total resistance of the circuit. The legend shows values of capacitors in μF.

Using Eq. (15) a simple criterion for inductance of the circuit without oscillations can be obtained:

$$L_c < \frac{C \times (R_c + ESR)^2}{4} - (ESL) \qquad (16)$$

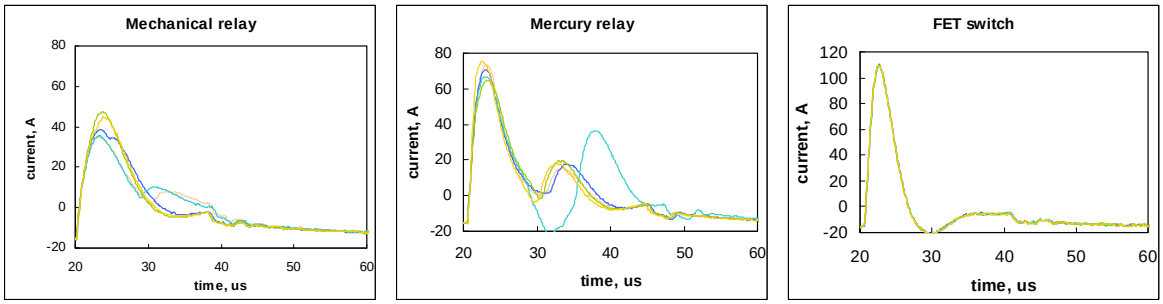
For example, for a 10 μF capacitor with ESR = 0.1 Ohm, ESL = 10 nH, and R_c = 0.6 Ohm, the inductance of the circuit, L_c, should be below 1,200 nH, which is relatively easy to implement. However, if C = 3 μF, the inductance should be below ~190 nH, which might present a challenge.

V.3. Type of switch.

Bouncing of contacts while turning on a mechanical switch can reduce and redistribute the energy of the transient into several current spikes, thus affecting the results of testing. As the bouncing is not reproducible, the results of such testing might vary from test to test. The MIL-

PRF-55365 standard does not pose any requirements on the quality of switching devices, and different researchers are using different types of switches: electronic switches (power FETs) [4] or mercury relays [8], which are considered as non-bouncing mechanical devices. As no requirements are set, some laboratories are using mechanical relays in spite of their notorious bouncing effect.

To evaluate the effect of switching devices used, three circuits have been developed. First, with a 25 A/240 V Potter and Brumfield mechanical relay, second, with a mercury 35 A relay (SMH100VN682M35X50T2), and third, with power FETs (four IRL2910 transistors with R_{DSON} = 0.026 Ohm connected in parallel). A 6,800 μF/100 V aluminum electrolytic capacitor with ESR = 0.037 Ohm was used as a bank capacitor, C_B, in the two latter circuits. In the first circuit a bank capacitor was made by eight 1 F/5.5 V SOHIO MAXCAP, LP-type capacitors connected in series (resulting in C_B = 125,000 μF). A 15 μF 50 V tantalum chip capacitor was stressed five times at a rated voltage consequently in all three set-ups without adding any limiting resistors. Measurements of ESR, C, and leakage currents (with an accuracy of 10 nA) verified the integrity of the part after each test. Oscillograms of current transients measured during these surge tests are shown in Figure 12.

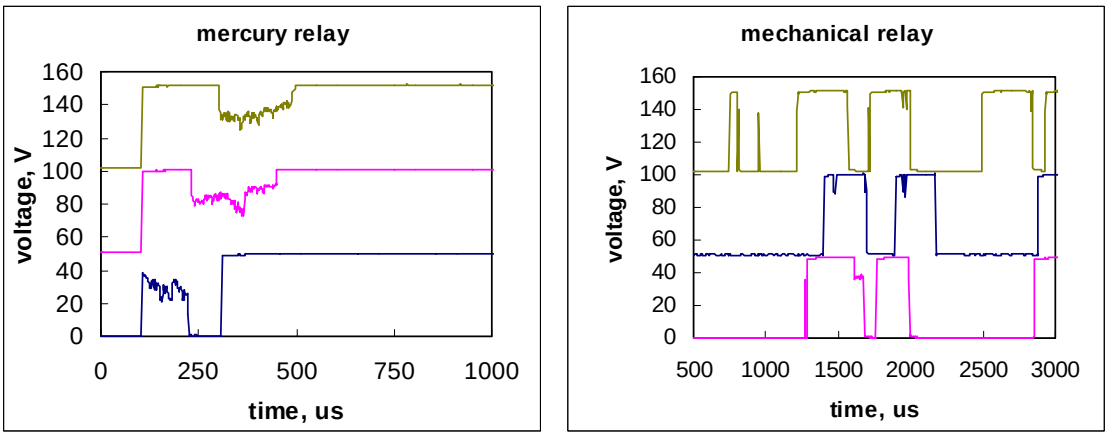


a) b) c)

Figure 12. Reproducibility of current spikes in three set-ups with different types of switches: mechanical relay (a), mercury relay (b) and power FETs (c). The same 15 μF/50 V tantalum capacitor was tested five times. No limiting resistors were used.

It is seen that the most reproducible results were obtained with the FET circuit. Both circuits with mechanical switches had significant variations in the shape of current spikes from test to test. The amplitude of spikes varied from 45 to 60 A for the circuit with a mechanical relay to 75 to 85 A for the circuit with a mercury relay, and to 110 A for the power FET circuit. This is most likely due to a decrease in both R_c and L_c in the row: the first, second, and third set-up.

To further evaluate the quality of switches used, oscillograms in set-ups with the mercury and mechanical relays were measured with a capacitor under test replaced with a power, low-inductance (~50 nH) 100-Ohm film resistor. Voltage transients measured across 100 Ohm resistors are shown in Figure 13.



a) b)

Figure 13. Voltage transients across a 100-Ohm resistor used as a replacement of capacitors in circuits with a mercury (a) and mechanical (b) relay. The curves are offset for better view of the transients.

The results confirm bouncing in both relays. However, bouncing in the mechanical relay was much more significant and manifested as a series of pulses stretching up to several milliseconds, whereas no pulses after a few hundred microseconds were observed in the mercury relay. This difference does not matter for surge testing of tantalum capacitors because of the short duration of the transients. For surge current testing, only bouncing, which occurs within the microsecond range, is important and for this reason mercury relays might perform as badly as mechanical relays.

V.4. Energy storage bank capacitor.

As Figure 12 shows, the amplitude of current spikes in the set-up with mechanical relay was approximately two times smaller than for a set-up with power FETs. One of the reasons for this is a large value of ESR of SOHIO MAXCAP capacitors, which according to the data sheet might exceed 1 Ohm. Connecting several of these capacitors in series increases the effective resistance of the circuit even further. This indicates the importance of limiting of the value of ESR of the bank capacitor and confirms the necessity to include this value in calculations of R_c. Aluminum electrolytic capacitors have low ESR values, and parts with large capacitances and voltages are readily available. This makes them good candidates for energy storage for the surge testing.

The purpose of using of the bank storage capacitor C_B is to simulate a power supply with a virtually unlimited current source so that the set voltage would be maintained constant during the test. When a capacitor C_B, which had been precharged to a voltage V_0, is discharged to a capacitor-under-test C, the charge initially stored in C_B will be distributed in two capacitors, C_B and C, and the resulting voltage after transient, V, would be lower than V_0:

$$V = V_0 \times \frac{C_B}{C_B + C}.$$

This allows estimation of the necessary value of C_B:

$$C_B = C \times \frac{\nu}{1-\nu}, \qquad (17)$$

where $\nu = V/V_0$ is a parameter indicating voltage stability during the test.

It is reasonable to require that the value of C_B is great enough so the voltage across the capacitor under test does not drop below ν = 95% to 99%. For this, the bank capacitor should be approximately 20 to 100 times greater than C. The existing requirement for C_B to be more than 50,000 μF is evidently excessive for tantalum capacitors of less than 500 μF, which is the majority of the parts employed in most applications.

Using excessively large energy storage bank capacitors might have negative consequences for surge current testing:

1. Connecting several capacitors with C << 50,000 μF in parallel increases the effective length of the wires and inductance of the circuit.
2. Connecting several capacitors with C >> 50,000 μF and low-rated voltage in series to increase the effective voltage of C_B also increases the inductance. Besides, it sums up ESR values, thus increasing resistance of the circuit, R_c.
3. To avoid damage to bank capacitors and/or power supplies, capacitor C_B is charged through a resistor R_{PS} (see Figure 5), which is presumably in the range from ~30 to 300 Ohms (assuming that 3 Ohms per volt is necessary to avoid damage to C_B and the rated voltage of the capacitor is in the range from 10 V to 100 V). At C_B = 50,000 μF the characteristic time of charging, $\tau = C_B \times R_{PS}$, varies from 1.5 sec. to 15 sec. In this case, for an initially discharged capacitor to be charged to 95% of the set voltage, the time of charging should exceed 3τ. This means that the charging time should be more than 4.5 to 45 sec., which is far greater than 4 seconds per MIL-PRF-55365. Maintaining the 4-second charging time in this case would significantly reduce the effective voltage and result in inadequate testing of the parts.

The necessity to maintain the rated voltage within ±5% limits during the testing by using large enough energy storage capacitors, instead of setting the minimal value of C_B, should be explicitly stated in the standard for the surge current testing.

V.5. Charging time.

MIL-PRF-55365 requires the charging time, τ_c = 4 seconds. As was shown above, in some cases this time might not be enough to fully charge the bank capacitor. Instead of setting a fixed charging time, it would be more reasonable to require that the charging time is sufficient enough to charge capacitor C_B to at least 95% of the nominal voltage. In the case when C_B is initially discharged, the following charging time is required:

$$\tau_c \geq 3 \times C_B \times R_{PS}. \qquad (18)$$

For the test circuit shown in Figure 5, much less time to restore the voltage on C_B might be necessary for cycles following the first one because normally, when no failure occurs, only a small portion of the charge will be lost. However, in cases when discharging of the capacitor under test occurs along with discharging of the bank capacitor, violation of condition (18) would decrease the effective voltage at which the test is performed.

Note that if the compliance current of the voltage power supply is set to a relatively low value, $I_{comp} < V_0/R_{PS}$, the current will not depend on R_{PS} and the necessary charging time should exceed

$\tau_{cc} = C \times V_0 / I_{comp}$. In this case, a use of Eq. (18) might result in a substantial decrease of the effective voltage during the test.

V.6. Discharging time.

The discharging time, τ_d, should be great enough to assure that the tantalum capacitor is discharged sufficiently (to 1 % of the rated voltage), so that the next current surge would be applied to a fully discharged capacitor and would be identical to the previous one. The discharge rate depends on the value of the resistor, R_d, used in the discharge path, and to assure that in a circuit shown in Figure 5 the voltage has dropped to 1% of the initial value, the necessary time can be calculated as:

$$\tau_d \geq 4.6 \times C \times (R_d + R_c) . \tag{19}$$

Even at rather large values of R_d of ~ 10 Ohm, τ_d is far below the required 4 seconds for capacitors up to 10,000 μF. Based on electrical conditions, even τ_d = 1 second would satisfy most practical cases.

Another reason, which might limit the minimum discharging time, is heating of the part during the consequent surge pulses. In the worst case (for overheating), when the value of discharge resistance R_d can be neglected compared to R_c, the same energy will be dissipated during the discharge portion of the cycle as during the charge portion. In this case the power dissipated during surge current testing at a frequency *f* can be calculated using the following simple equation:

$$P = 2 \times Q \times f = \alpha \times C \times V^2 \times f , \tag{20}$$

Assuming that the capacitor has temperature resistance R_t, the temperature increase can be calculated as:

$$\Delta T = \alpha \times C \times V^2 \times f \times R_t . \tag{21}$$

This equation allows for estimation of the maximum frequency of testing, which would increase the temperature below the acceptable level of ΔT_a:

$$f = \frac{1}{\tau_c + \tau_d} < f_{\max} = \frac{\Delta T_a}{\alpha \times C \times V^2 \times R_t} . \tag{22}$$

According to Salisbury [22], the thermal resistance of tantalum capacitors in free air conditions varies from 185 to 236 ^{o}C/W. Based on these data and assuming ΔT_a = 1 ^{o}C, Figure 14 shows results of calculations of f_{max} for surge testing in the case, when R_c = 0.6 Ohm and α = 0.14, at two voltage conditions of 10 V and 50 V. It is seen that at relatively low voltages (10 V and below) the frequency of testing required per MIL PRF-55365 (1/8 Hz) complies with the requirements Eq. (22) for most practical cases, up to 1,000 μF. However, for high-capacitance high-voltage parts, overheating is possible and testing at frequencies below 0.125 Hz might be necessary.

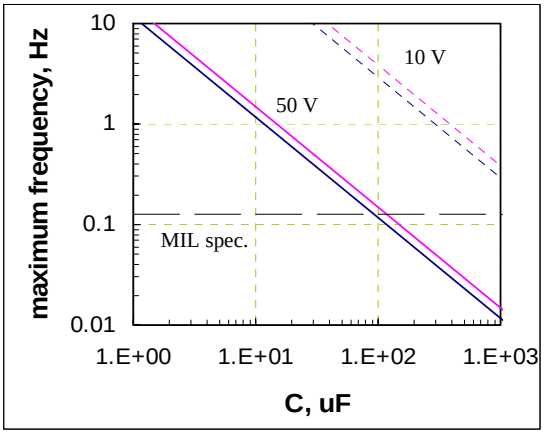


Figure 14. Comparison of maximum frequency of surge current testing and MIL standard requirements (black dashed line).

Similar analysis resulting also in equation (20) was used by Reed [23] to estimate thermal effects of high ripple and/or surge currents in tantalum capacitors. He found strong agreement between the model and experimental data, when the temperature of 10 μF/35 V capacitors was raised to ~ 85 ^{o}C at a relatively high (140 A) surge current pulses at a frequency of cycling of 93 Hz. Our experiments with 15 μF/50 V capacitors during surge current testing at a frequency of 1 Hz with I_{sp} ~ 170 A showed that the temperature increase did not exceed 1 ^{o}C, which is in agreement with results of calculations shown in Figure 14.

Based on Eq. (22) and assuming ΔT_a = 1 ^{o}C, a condition for the necessary discharge time can be obtained:

$$\tau_d > \alpha \times C \times V^2 \times R_t - \tau_c . \qquad (23)$$

Considering also the requirement to discharge the capacitor to 1% of the rated voltage, it is reasonable to demand that the duration of discharge cycle should be 1 second or per Eq. (23), whichever is larger.

VI. Conclusions.

- Inductance of tantalum capacitors, ESL, and especially elements of the circuit used for surge current testing, L_c, might significantly affect the shape and amplitude of the current and voltage transients. Voltage overshooting up to 100% of the rated voltage might occur at large enough values of L_c, causing failures due to breakdown of tantalum pentoxide dielectric of the capacitors.
- Inductance of the circuit should be limited to avoid overshooting, reduce variations of the current spike shape, and assure reproducible results of the testing. The condition per Eq. (14) can be used to estimate maximum acceptable inductance for a given capacitor and test conditions.
- According to the existing specifications only maximum value of the resistance of the circuit is limited. This might result in unacceptably high variations of the portion of energy dissipated in the capacitor in different set-ups used for the testing. To make test results more

reproducible and to relax requirements for inductance of the circuit, it is reasonable to tighten the limits for the resistance to the range from 0.5 to 1 Ohm. The value of R_c should be estimated using a surge current oscillogram and reported together with the results of surge current testing for reference purposes.

- The reproducibility of transients in three surge current test set-ups with different types of switching devices, a mechanical relay, a mercury relay, and a power FET, have been evaluated. Both mechanical devices exhibited contact bouncing, and the best reproducibility of current transients was achieved with power FETs.
- The requirements for the energy storage bank capacitor and duration of charge/discharge cycles are discussed. Simple equations are suggested to estimate the necessary C_B, τ_c, and τ_d values to maintain adequate and reproducible conditions of the testing.

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